Simulation Standard

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HiSIM Methodology for the Parameter Extraction in Accordance with the Model Derivation

I. Introduction

HiSIM (Hiroshima university STARC IGFET Model) is one of the surface potential based Spice models [1], [2] and pioneered the iterative approach to obtain the surface potential applicable in compact models. The model aims for MOSFET technology of 100 nm or below. The parameter extraction procedure was introduced first by the model developers: Semiconductor Technology Academic Research Center (STARC) [3], [4]. Silvaco ***UTMOST-III*** introduced the first version of the local optimization strategies for HiSIM-1.1 in 2002 [5]. Since then, the parameter extraction methodology has been reviewed thoroughly. This article is meant to provide significant aspects on the HiSIM version 1.2 parameter extraction for ***UTMOST-III*** users.

Since the surface potential is obtained by solving Poisson equation, and the geometric effects are directly related to the electric field calculated from the potential, establishing the HiSIM model parameter extraction methodology forces traditional SPICE modeling engineers to refresh their understanding of device physics. Moreover, making the HiSIM model to be scalable over the wide geometric region challenges the experienced manner of this tradition. In this paper, each step of the developed HiSIM model parameter extraction is discussed from the model derivation point. The model parameters are symbolized with the capital, bold and italic letters. Also, the HiSIM-1.2 equations and the numbers used herein are based on HiSIM1.2.0 user's manual [3]. The detailed ***UTMOST-III*** local optimization strategies with the practical application results will be covered in a future edition of simulation standard issued by Silvaco International.

II. HiSIM Methodology

A. Substrate Model Parameters

MOSFET threshold voltage parameter (Vth) is very popular in MOSFET Spice models such as in the Level-1, 2, 3 and in the UC Berkeley BSIM3 models. The threshold voltage parameter extraction comes at the very first of the extraction procedures. In contrast, HiSIM calculates the surface potential by applying Poisson equation to the channel region and the potentials are used for the drain current computation with no explicit threshold voltage parameter. The followings are the HiSIM formulas of the drain current with the surface potentials.

$$I_{\rm ds} = \frac{W_{\rm eff}}{L_{\rm eff}}\mu\frac{IDD}{\beta}$$

$$\begin{aligned} IDD = {} & C_{\rm ox}(\beta V'_{\rm G}+1)(\phi_{\rm SL}-\phi_{\rm S0}) - \frac{\beta}{2}C_{\rm ox}(\phi^2_{\rm SL}-\phi^2_{\rm S0}) \\ & - \frac{2}{3}\left(qN_{\rm sub}L_{\rm D}\sqrt{2}\right)\left[\left\{\beta(\phi_{\rm SL}-V_{\rm bs})-1\right\}^{\frac{3}{2}}\right. \\ & \left. - \left\{\beta(\phi_{\rm S0}-V_{\rm bs})-1\right\}^{\frac{3}{2}}\right] \\ & + (qN_{\rm sub}L_{\rm D}\sqrt{2})\left[\left\{\beta(\phi_{\rm SL}-V_{\rm bs})-1\right\}^{\frac{1}{2}}\right. \\ & \left. - \left\{\beta(\phi_{\rm S0}-V_{\rm bs})-1\right\}^{\frac{1}{2}}\right] \end{aligned} \quad (23)$$

$$C_{\rm ox} = \frac{\epsilon_{\rm ox}}{T_{\rm ox}} \quad (11)$$

$$V'_{\rm G} = V_{\rm gs} - V_{\rm fbc} + \Delta V_{\rm th} \quad (12)$$

$$\beta = \frac{q}{kT} \quad (13)$$

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R} + \Delta V_{\rm th,P} + \Delta V_{\rm th,W} - \phi_{\rm Spg} \quad (73)$$

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V_{th} represents the threshold voltage shifts referring to the long channel device including the short channel (ΔVth,SC), the reverse short channel ($V_{th,R}$ and $V_{th,P}$), and the reduced channel width ($V_{th,W}$) effects. Most of them are related to the electric field gradients for the lateral direction.

Therefore, the substrate parameters such as the substrate impurity concentration (***NSUBC***), the flat-band voltage (VFBC), the maximum pocket concentration (***NSUBP***), and the pocket penetration length (***LP***) are to be determined first. At the same time, the oxide thickness (***TOX***) is also to be fixed as the source of the vertical electric field.

$$N_{\rm sub} = \frac{N_{\rm subc}(L_{\rm eff} - L_{\rm p}) + N_{\rm subp}L_{\rm p}}{L_{\rm eff}} \quad (39)$$

Effective impurity concentration used in the HiSIM equation is the averaged value using ***NSUBC***, ***NSUBP***, and ***LP*** parameters (eq.39). The eq.39 was supposed to limit the ***LP*** value less than the Leff value. However, the formula enables it become larger than the Leff. There is no structural constraint, which was found through the trial parameter extraction applied for 90 nm technology [6]. For long and wide channel devices, the ***NSUBP*** and ***LP*** have less influence and the initial value determination appears to be arbitrary. But, the ***LP*** must be defined and the remaining substrate parameters should be extracted under the fixed value at the first step of the extraction. The reasonable approach to define the LP is under investigation.

The ***TOX*** requires a capacitance voltage curve (CGG) for the determination. The substrate related parameters could be fixed using Ids versus Vgs curve for the large geometry transistor. Also, the capacitance curve could be appropriate for the initial value findings. Naturally, gate current contribution must be considered for very thin gate oxide devices.

With those initial values, the sub-threshold drain current region is used for the substrate parameter optimization. Since HiSIM has no body effect coefficient parameters like in the previous generation models, the substrate parameter determination at the very first stage almost destines the body bias behavior of the HiSIM model.

B. Carrier Mobility: Low Field Mobility

HiSIM low field mobility model follows the mobility universality [7]. Three scattering mechanisms such as Coulomb, phonon, and surface roughness effects are taken into account.

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \quad (50)$$

$$\mu_{\rm CB}({\rm Coulomb}) = MUECB0 + MUECB1\frac{Q_{\rm i}}{q \times 10^{11}} \quad (51)$$

$$\mu_{\rm PH}({\rm phonon}) = \frac{MUEPH1}{(T/300{\rm K})^{MUETMP} \times E_{\rm eff}^{MUEPH0}} \quad (52)$$

$$\mu_{\rm SR}({\rm surface\ roughness}) = \frac{MUESR1}{E_{\rm eff}^{MUESR0}} \quad (53)$$

The gate bias region of Ids versus Vgs should be properly selected with this mobility universality in mind for the parameters (***MUECB0, MUECB1, MUEPH1, MUESR1***) using the wide channel width and the long channel length (large) device. Although the target I-V curve for the large device is easily expressed with the rough bias selections, the scalable model would become difficult to be achieved. Some parameters are related with the electric field component. The low field mobility characterization with split C-V method might provide an insight for the bias selection.

In addition, the surface roughness effect might be indistinguishable from the HiSIM pocket resistance parameter effect. The Ids degradation at the high Vgs could be expressed only with the surface roughness parameter. However, it might be an overestimation of the decreasing mobility. And the short channel length devices might show the smaller Ids current for the target curves.

C. Geometric Effects: Reverse Short Channel Effect

HiSIM geometric effects toward the MOS channel length such as the reverse short channel (RSC) and the standard short channel (SC) effects need the careful approach. The HiSIM RSC expression is based on the impurity inhomogeneity in the lateral direction and the lateral electric field strength is modified as following.

$$\Delta V_{\rm th,P} = (V_{\rm th,R} - V_{\rm th0})\frac{\epsilon_{\rm Si}}{C_{\rm ox}} W_{\rm d} \frac{dE_{y,\rm P}}{dy} \quad (35)$$

$$V_{\rm th,R} = V_{\rm fbc} + 2\Phi_{\rm B} + \frac{\sqrt{2qN_{\rm sub}\epsilon_{\rm Si}(2\Phi_{\rm B} - V_{\rm bs})}}{C_{\rm ox}} \quad (36)$$

$$V_{\rm th0} = V_{\rm fbc} + 2\Phi_{\rm BC} + \frac{\sqrt{2qN_{\rm subc}\epsilon_{\rm Si}(2\Phi_{\rm BC} - V_{\rm bs})}}{C_{\rm ox}} \quad (37)$$

$$\frac{dE_{y,\rm P}}{dy} = \frac{2(V_{\rm bi} - 2\Phi_{\rm B})}{PARL1 \cdot L_{\rm p}^2}\left(SCP1 + SCP2 \cdot V_{\rm ds} + SCP3 \cdot \frac{2\Phi_{\rm B} - V_{\rm bs}}{L_{\rm p}}\right) \quad (38)$$

The four model parameters such as ***PARL1, SCP1, SCP2***, and ***SCP3*** in addition to the substrate related parameters (***NSUBC, NSUBP***, and ***LP***) are included in the equation.

$$N_{\rm sub} = \frac{N_{\rm subc}(L_{\rm eff} - L_{\rm p}) + N_{\rm subp}L_{\rm p}}{L_{\rm eff}} \quad (39)$$

The ***NSUBP*** under the fixed ***LP*** should be mainly used to express a shift of Ids versus Vgs curve to the larger Vgs (Vth roll-up) of the RSC devices. And it should be modified carefully to have the small effect on the SC device curves. Too much change on the SC device characteristics at this step means the shift of Ids versus Vgs toward the smaller Vgs (Vth roll-off) couldn't be expressed later with any effort. It means the pre-defined ***LP*** is too small

to assign the larger contribution to the ***NSUBP*** for the averaged Nsub. The ***LP*** must be redefined, other substrate parameters also must be extracted according to the previous description. So that the ***NSUBP*** value could become reasonable compared to the ***NSUBC***, and the RSC effect could be expressed clearly [8].

One of remaining four parameters, ***PARL1***, is fixed to unity. ***SCP1*** appears to be used for the slight tuning of the RSC effect expression. And ***SCP3*** could be used to modify the body bias effect for the RSC devices. Finally, ***SCP2*** which relates the RSC effect with the drain bias needs to be optimized for Ids versus Vgs under the saturation condition.

D. Geometric Effects: Standard Short Channel Effect

The standard short channel effect is expressed with the similar formula for the reverse short channel effect.

$$\Delta V_{\mathrm{th,SC}} = \frac{\epsilon_{\mathrm{Si}}}{C_{\mathrm{ox}}} W_{\mathrm{d}} \frac{dE_y}{dy} \tag{28}$$

$$W_{\mathrm{d}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}(2\Phi_{\mathrm{B}} - V_{\mathrm{bs}})}{qN_{\mathrm{sub}}}}. \tag{29}$$

$$\frac{dE_y}{dy} = \frac{2(V_{\mathrm{bi}} - 2\Phi_{\mathrm{B}}')}{PARL1(L_{\mathrm{eff}} - PARL2)^2} \left(SC1 + SC2 \cdot V_{\mathrm{ds}} + SC3 \cdot \frac{2\Phi_{\mathrm{B}} - V_{\mathrm{bs}}}{L_{\mathrm{eff}}} \right) \tag{30}$$

$$\Phi_{\mathrm{B}}' = \Phi_{\mathrm{B}} + PTHROU \cdot \left(\Phi_{\mathrm{B}}''(V_{\mathrm{gs}}) - \Phi_{\mathrm{B}} \right) \tag{31}$$

However, such four parameters as ***PARL2***, ***SC1***, ***SC2***, and ***SC3*** should be optimized carefully to obtain the standard short channel (SC) effect. ***PARL2*** has the length dimension, modifies the effective channel length used in the SC effect equation and shows much influence on the effect. ***SC1*** parameter has also the great effect to pull the overshot Ids versus Vgs curves resulted by the RSC expression toward the Vth roll-off (SC effect) direction. Also, ***SC2*** influences the higher drain bias region of Ids versus Vgs curves, and expresses the SC effect dependency on the drain bias. The extraction of the standard short channel parameters requires the software optimizer to be used with much care. Especially, both the ***SC1*** and ***SC2*** values spread widely between 0 and 200 depending on the device characteristics of RSC and SC effects.

E. Carrier Mobility: High Field Mobility

Now that such parameters as the substrate, the low field mobility and the RSC and SC effect parameters are fixed using the Ids versus Vgs at the low Vds, HiSIM high field mobility parameters should be extracted. The HiSIM high field mobility is obtained by modifying the low field component with the lateral electric field in association with the modulated maximum velocity parameter.

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\mathrm{y}}}{V_{\mathrm{max}}} \right)^{BB} \right)^{\frac{1}{BB}}} \tag{60}$$

$$V_{\mathrm{max}} = \frac{VMAX}{1.8 + 0.4(T/300\mathrm{K}) + 0.1(T/300\mathrm{K})^2} \tag{61}$$

$$V_{\mathrm{max}} = \frac{V_{\mathrm{max}}}{1 - \frac{VOVER}{L_{\mathrm{eff}}^{VOVERP}}} \tag{62}$$

The HiSIM maximum velocity (***VMAX***) modulation adopts a nonlinear expression with two model parameters which are related to the channel length. The lateral electric field is also the function of channel length. Therefore, the high field mobility dependency on the channel length could become complex and hard to be predicted. Therefore, tuning over the wide range of the channel length would be the most critical step to obtain the scalable model parameters over the channel length.

In order to trace the drain bias influence, Ids versus Vgs curves under the various drain voltages appear to be suitable as the target characteristics for the parameter optimization. Whether the equation could be capable of depicting the scalability for 100 nm below technology, or not, requires the verification with various technology devices.

F. Geometric Effects: Narrow Width Effect

HiSIM-1.2 narrow width effect description which takes the shallow trench isolation (STI) technology into account looks simple, and has waited for the validation using the actual and practical devices.

$$\Delta V_{\mathrm{th,W}} = \left(\frac{1}{C_{\mathrm{ox}}} - \frac{1}{C_{\mathrm{ox}} + 2C_{\mathrm{ef}}/(L_{\mathrm{eff}} W_{\mathrm{eff}})} \right) qN_{\mathrm{sub}} W_{\mathrm{d}} \tag{71}$$

$$C_{\mathrm{ef}} = \frac{2\epsilon_{\mathrm{ox}}}{\pi} L_{\mathrm{eff}} \ln \left(\frac{2T_{\mathrm{fox}}}{T_{\mathrm{ox}}} \right) = \frac{WFC}{2} L_{\mathrm{eff}} \tag{72}$$

A trial report on this methodology reveals the effectiveness of HiSIM approach [6].

G. Geometric Effects: Wide Width Effect

The second STI effect expression in HiSIM-1.2 is the mobility reduction assuming the STI induced mechanical stress. The wider device is supposed to suffer the mobility degradation.

$$MUEPH1 = MUEPH1 + MUEPH2 \cdot \log(W_{\mathrm{gate}}) \tag{72}$$

$$\log(W_{\mathrm{gate}}) \geq W0$$

H. Geometric Effects: Hump in Sub-Threshold Current

Another STI induced effect in HiSIM-1.2 is the drain current hump in the sub-threshold region. As far as the parameter extraction for the varied channel length is concerned, further validation seems to be required.

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Behavioral Modeling of PLL Using Verilog-A

Introduction

In this article, we describe practical behavioral modeling for highly non-linear circuits using Verilog-A, which is analog extension of Verilog-AMS. At first, we describe behavioral modeling techniques for phase/frequency detectors (PFD) and voltage-controlled oscillators (VCO) those are essential part of phase-locked loop systems shown in Figure.1. Model parameter extraction techniques are described and demonstrated later. Finally, these models are simulated with SmartSpice and verified against the results of transistor circuit simulations.

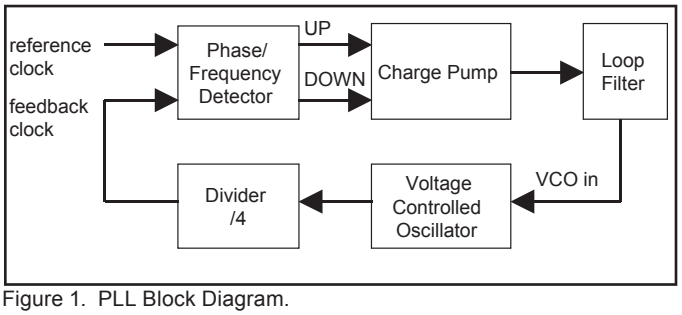

Figure 1. PLL Block Diagram.

Phase Detector (PD)

A well-known sequential-logic PFD shown in Figure.2(a) is used for phase/frequency detection circuit. This PFD produces UP and DOWN signals depending on the phase difference between reference clock and feedback clock (Figure.2(b)).

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The behavioral model of PFD can be represented as shown in List.1. This module monitors the phase difference between the clocks. When the rising edge of REF clock occurs before the rising edge of FB clock, the module activate UP signal and then forces the VCO to increase the oscillation frequency. In the reverse case, the module activate DOWN signal and forces the VCO to decrease the frequency. Note that UP and DOWN signal are active-low and active-high respectively.

List 1. Behavioral representation of PFD in Verilog-A

```
module  pll_pd  (ref_clk, fb_clk, up_out, down_out);
inout   ref_clk, fb_clk, up_out, down_out;
electrical  ref_clk, fb_clk, up_out, down_out;
parameter  real  vdd=3.3,
                 ttol=10f,
                 ttime=0.2n ;
integer  state;        // state=1 for down, -1 for up
real       td_up, td_down ;
```

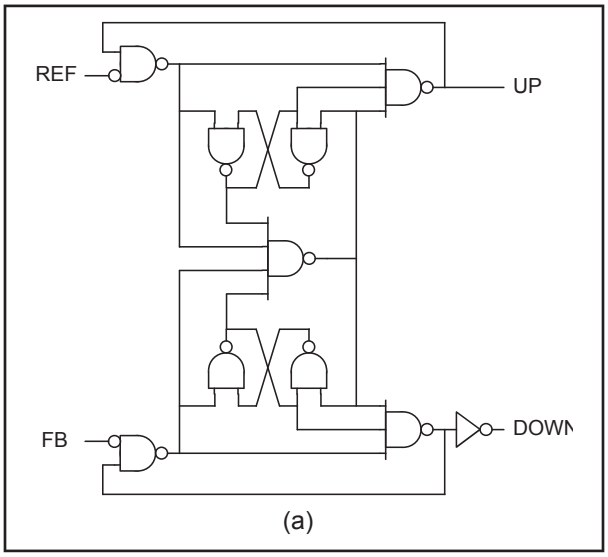

Figure 2a. PFD circuit.

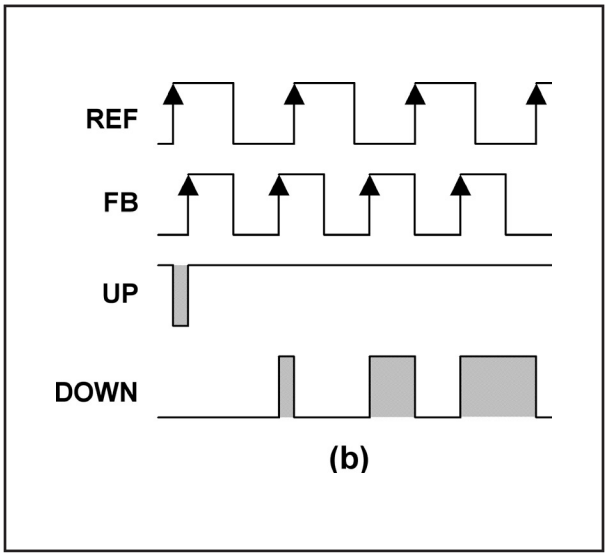

Figure 2b. Basic operation.

```
analog  begin
    @(cross( V(ref_clk) - vdd/2 , 1 , ttol ))  begin
    state = state - 1;
    if(V(up_out)>vdd/2)   td_up=480p; else  td_up=1005p;
    if(V(down_out)<vdd/2) td_down=480p; else td_down=1090p;
end
@(cross( V(fb_clk) - vdd/2 , 1 , ttol ))  begin
    state = state + 1;
    if(V(up_out)>vdd/2)   td_up=480p; else  td_up=1005p;
    if(V(down_out)<vdd/2)  td_down=480p;  else  td down=1090p;
 end

    if ( state > 1 ) state = 1 ;
    if ( state < -1 ) state = -1;
    V(down_out) <+ transition( (state + 1)/2*vdd , td_down , ttime );
    V(up_out) <+ transition( (state - 1)/2*vdd+vdd , td_up , ttime );
    end
endmodule
```

In this module, we use td_up and td_down variables to define delay time of input-to-UP and input-to-DOWN respectively. Since delay time of rise transition is different from fall transition, different values should be assigned to these variables depending on output transition direction. The following codes used in the module allow designers to define different delay time for rise and fall transition independently.

```
if(V(up_out)>vdd/2) td_up=480p;   else  td_up=1005p;
if(V(down_out)<vdd/2)  td_down=480p; else td_down=1090p;
```

The optimal value of variables can be obtained from transistor level simulation shown in Figure.3 (a) and (b). From these plots, we can obtain the optimal value of td_up=480ps when rising and td_up=1005ps when falling, and td_down=480ps when rising and td_down=1090ps when falling. By using these optimal values, we can see good agreement in the output waveforms of both transistor level and Verilog-A simulations.

Voltage Controlled Oscillator (VCO)

An ideal voltage-controlled oscillator generates a periodic output signal whose frequency is a linear function of control voltage. The output frequency fout can be expressed as;

$$fout = fnom + gain*Vcont$$

where fnom is a nominal(or free running) frequency, gain is the gain of VCO in Hz/V, and Vcont is a control voltage supplied from charge pump. Since phase is the time-integral of frequency, the sinusoidal output of VCO can be expressed as;

$$Vout(t) = A*sin(2*phi*integral(out)) + Voffset$$

where A is a amplitude of sinusoidal and Voffset is an output offset voltage.

With based on the above principle, behavioral model of VCO can be represented as shown in List.2.

List 2. Behavioral representation of VCO in Verilog-A

```
module  pll_vco  ( in, out ) ;
inout       in, out ;
electrical  in, out ;
parameter  real vdd = 3.3,   // operational voltage
                amp = vdd/2,     // amplitude of vout
                offset = vdd/2,   // offset of vout
                gain = 540e6,    // gain  [Hz/V]
                vnom = 1.27,     // nominal vin
                fnom = 400e6;   // frequency at vnom

        real        freq ;

        analog  begin
            freq = fnom + gain*(V(in) - vnom) ;
            V(out)  <+  amp*sin(2*`M_PI*idt(freq)) + offset ;
        end
endmodule
```

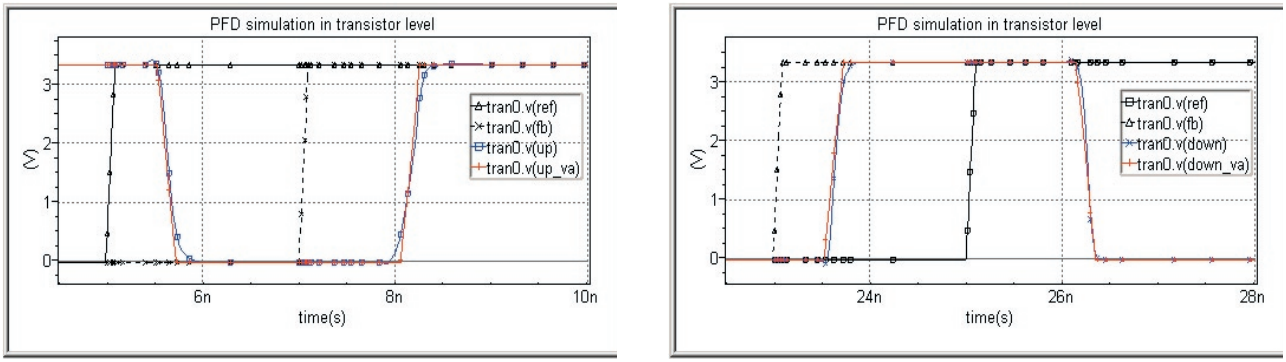

Figure 3. Simulation results of PFD. Shown are (a) UP waveforms, and (b) DOWN waveforms.

Note that, Vcont is replaced by V(in)-vnom in the module description.

The module parameters fnom is the nominal frequency and is defined in design specification. The 'offset' may be defined as half of VDD. The vnom and gain should be extracted from transistor level simulation. Figure.4 shows the transistor level simulation result of VCO frequency respect to control voltage. vnom can be found by measuring control voltage at which VCO frequency is equal to 400MHz, and gain can be obtained by calculating the gradient of the curve at Vcont=vnom. In this example, we obtained vnom=1.27v and gain=540MHz/V from the plot.

Verilog-A simulation result is also displayed in Figure.4. Since we assume the VCO gain is a linear function of control voltage, there's a discrepancy in low and high regime of Vcont. However, you can overcome this issue by adapting non-linear function for gain expression.

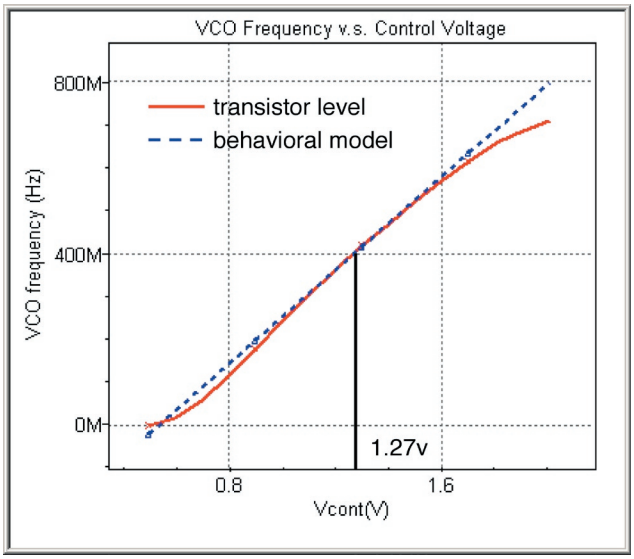

Figure 4. Simulation results of VCO.

Conclusion

By using behavioral modeling technique, and a mixed signal simulation with SmartSpice, PLL system can be efficiently simulated with good accuracy and reasonable run-time cost. The module characteristic can be parameterized in behavioral representation, and the parameters can be easily extracted from the transistor level simulation. A designer would thus start the design process by using an all behavioral model of PLL and focusing on optimizing module parameters. Once enough performance is obtained, the modules can be widely used for various subsystems and in a mixed signal simulations in future designs.

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V. Summary

The methodology on HiSIM-1.2 model parameter extraction was discussed from the model derivation point. HiSIM-1.2 incorporates other effects such as Poly-Depletion, Quantumn-Mechanical, Channel-Length Modulation, etc.. The readers of interest should refer to HiSIM-1.2.0 user's manual [3]. The practical procedure was applied to the actual N-channel MOS devices and the HiSIM-1.2 model parameter set was obtained. The simulated result demonstrated the geometrical scalability down to 100 nm from 10 um channel length with no binning at all. The UTMOST-III local optimization strategies with the applied result will appear on a future issue of Simulation Standard from Silvaco International.

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Accounting for Shallow-Trench-Isolation (STI) Effects in BSIM4 and HiSIM MOSFET Models

1. Introduction

Semiconductor devices are continuously improved with regard to intrinsic characteristics, as well as reduced geometries. Among all requirements, there is a need for an efficient device isolation technique as CMOS technologies are scaled down below the 0.25μm generation. Shallow Trench Isolation (STI) has become an essential isolation scheme as a replacement for LOCal Oxydation of Silicon (LOCOS). It allows reaching a higher packing density, tighter design rules, lower parasitics and higher yields. However, the basic STI process sequence involves several sources of mechanical strain, which can significantly increase the stress levels in the enclosed silicon area (Figure 1). It was shown that this stress in turn influences junction leakage but also MOS electrical characteristics. There are several ways to account for the effect of STI-induced stress in standard compact models. The purpose of this article is to present two different approaches developed by the universities of Berkeley and Hiroshima. In both cases, new equations were derived and new parameters have been introduced in the latest versions of BSIM4 and HiSIM compact models. These new versions are currently supported by Silvaco ***SmartSpice/UTMOST*** softwares.

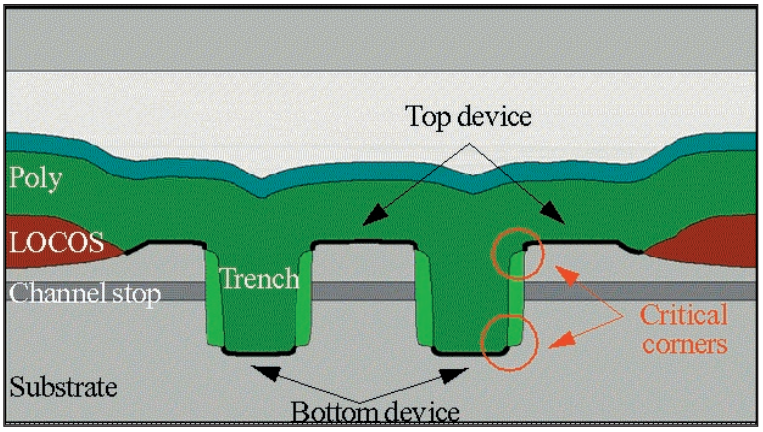


Figure 1. Mechanical stress induced by STI process.

2. HiSIM STI Model Equations

HiSIM is a MOSFET model developped by Hiroshima University, started in 2001. The equations for the STI effect were added in version 1.1 and account for two major STI effects experimentally observed on I-V characteristics:

- a "double hump" in the Id/Vg characteristic (subthreshold region),
- a lower threshold voltage value.

The edge of the trench has an influence on the electric field. The impurity concentration and the oxyde thickness are different from those at the middle of the width. Therefore, a modified surface potential is computed. Since the threshold voltage for the corresponding leakage current is different from the threshold voltage of the main current, the STI effects can be observed only in the sub-threshold region.

The local modified surface potential is computed using the expression shown in equation 1.

These equations are based on the assumption that the current in the subthreshold region is mainly due to diffusion. The carrier concentration, $Q_{N,STI}$, is calculated analytically using the Poisson equation, with a dedicated substrate impurity concentration N_{STI}. The *WVTHSC* parameter is used to discriminate the short-channel threshold characteristics of the edge from the intrinsic part.

The final equation is shown in equation 2.

The *WSTI* parameter represents the width of the high-field region.

$$\Phi_{S,STI} = V'_{gs,STI} + \frac{\varepsilon_{Si} \cdot Q_{N,STI}}{C^2_{ox}} \left[1 - \sqrt{1 + \frac{2C^2_{ox}}{\varepsilon_{Si} \cdot Q_{N,STI}} \left(V'_{gs,STI} - V_{bs} - \frac{1}{\beta} \right)} \right]$$

with

$$V'_{gs,STI} = V_{gs} - V_{fb} + V_{th} \cdot WVTHSC$$

Equation 1.

$$I_{ds,STI} = 2 \cdot \frac{W_{STI}}{L_{eff} - \Delta L} \cdot \mu \cdot \frac{Q_{N,STI}}{\beta} [1 - \exp(-\beta \cdot V_{ds})]$$

Equation 2.

An example of the I-V characteristics is shown on Figure 2. It is important to note that unrealistic parameter values are used to make the "double hump" and the lower threshold voltage visible. For most practical situations, the effect on I-V characteristic is not so important and may be negligeable with optimized STI processes.

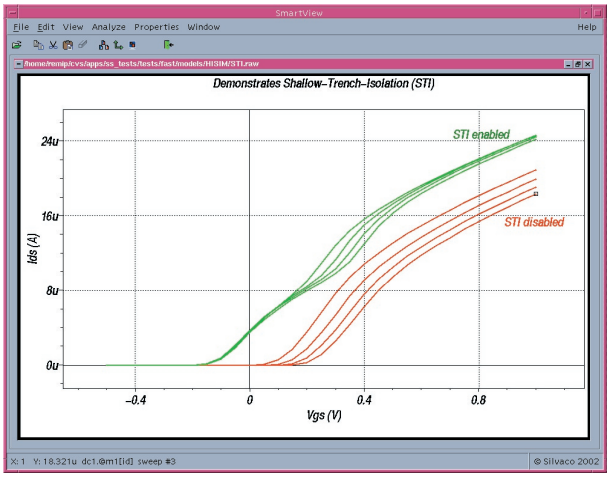


Figure 2. STI-induced stress effect on Id-Vg characteristics.

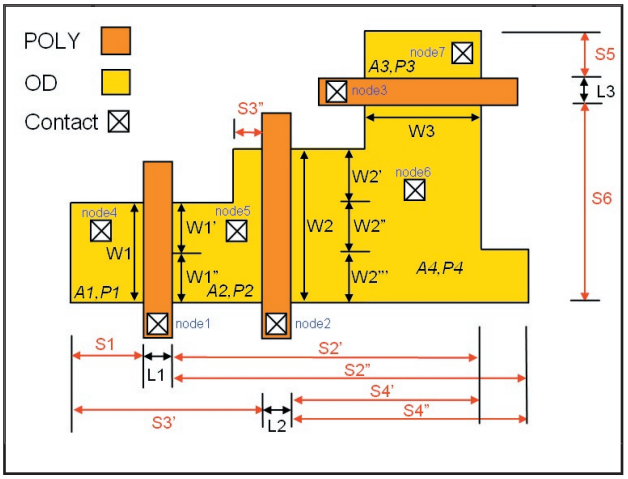


Figure 3. Irregualr LOD device geometry parameters.

3. BSIM4 STI Model Equations

The approach chosen by the University of Berkeley is based on the observation that the mechanical stress induced by STI makes MOSFET performance depend on the active area size, as well as the location of the device in the active area. The effect of stress on mobility and saturation velocity was experimentally demonstrated. A phenomenological model was derived and introduced in BSIM4v3.0 to consider the influence of stress on mobility, velocity saturation, threshold voltage, body effect and DIBL effect.

In the Silvaco implementation of BSIM4, several stress effect models can be invoked by specifying the model parameter STIMOD. This selector was not supported in the original Berkeley release of BSIM4v3.0. As STI effect is turned off by default, it is supported for all versions of BSIM4.

- STIMOD=0

Stress effect turned off.

- STIMOD=1 (Berkeley model introduced in BSIM4.3.0 beta of December 2002) If instance parameters SA, SB are set to positive values with NF=1 or if SA, SB, SD are all set to positive values with NF>1 and the model parameter SK0 is also set to a positive value, the mobility *U0(T)*and the carrier velocity *VSAT(T)* account for changes due to stress effect and are expressed as shown in Equation 3.
- STIMOD=2 (TSMC model for irregular LOD devices) This model corresponds to the Berkeley model (STIMOD=3) with different expressions for the intermediate variables Inv_sa and Inv_sb. These latter ones are computed as functions of instance parameters SA1...SA10, SB1...SB10 and SW1...SW10 to account for irregular LOD devices. NF must be unspecified or set to 1 to allow stress effect computation if STIMOD=2 is invoked. (Equation 4.)
- STIMOD=3 (Berkeley model for multi-finger devices) This model was introduced by Berkeley in the final release of BSIM4.3.0 of May 9th 2003. It considers the influence of stress on mobility, velocity saturation, threshold voltage, body effect and DIBL effect by modifying the parameters shown in Equation 5.

The TSMC model was developed to account for devices with irregular oxide definition (Figure 3). Berkeley models must be used for multi-finger devices (Figure 4). If only SA (or SA1) and SB (or SB1) are specified with NF=1, STIMOD=2 and STIMOD=3 models are equivalent.

$$U0'(T) = \frac{U0(T)}{1+\rho} \quad \text{and} \quad VSAT'(T) = \frac{VSAT(T)}{1+K\cdot\rho}$$

where

$$\rho = SK0\cdot\left[\rho'\cdot\frac{\sinh\left(\frac{NF}{2\cdot SL}\cdot(SD+L)\right)}{NF\cdot\sinh\left(\frac{SD+L}{2\cdot SL}\right)} + \frac{SK2}{W}\cdot\exp\left(-\frac{W}{SW}\right)\right]$$

$$\rho' = \left(1+\frac{SK1}{LOD}\right)\cdot\left(\exp\left(-\frac{SA+D}{SL}\right)+\exp\left(-\frac{SB+D}{SL}\right)\right)\cdot\frac{\sinh\left(\frac{L_{eff}}{2\cdot SL}\right)}{\frac{L_{eff}}{2\cdot SL}}$$

$$D = 0.5\cdot(NF\cdot L+(NF-1)\cdot SD)$$

$$LOD = SA+SB+2\cdot D$$

Equation 3.

$$\text{Inv_sa} = \sum_{i=1}^{10}\frac{SW_i}{W}\cdot\frac{1}{SA_i+0.5\cdot L} \quad \text{and} \quad \text{Inv_sb} = \sum_{i=1}^{10}\frac{SW_i}{W}\cdot\frac{1}{SB_i+0.5\cdot L}$$

Equation 4.

$$U0'(T) = U0(T) \cdot \frac{1+\rho}{1+\rho_{ref}}$$

$$VSAT'(T) = VSAT(T) \cdot \frac{1+\mathrm{KVSAT}\cdot\rho}{1+\mathrm{KVSAT}\cdot\rho_{ref}}$$

$$VTH0'(T) = VTH0(T) + \frac{\mathrm{KVTH0}}{\mathrm{Kstress_vth0}} \cdot (\mathrm{Inv_sa} + \mathrm{Inv_sb} - \mathrm{Inv_sa_ref} - \mathrm{Inv_sb_ref})$$

$$K2'(T) = K2(T) + \frac{\mathrm{STK2}}{\mathrm{Kstress_vth0}^{LODK2}} \cdot (\mathrm{Inv_sa} + \mathrm{Inv_sb} - \mathrm{Inv_sa_ref} - \mathrm{Inv_sb_ref})$$

$$ETA0'(T) = ETA0(T) + \frac{\mathrm{STETA0}}{\mathrm{Kstress_vth0}^{LODETA0}} \cdot (\mathrm{Inv_sa} + \mathrm{Inv_sb} - \mathrm{Inv_sa_ref} - \mathrm{Inv_sb_ref})$$

where

$$\rho = \frac{\mathrm{KU0}}{\mathrm{Kstress_u0}} \cdot (\mathrm{Inv_sa} + \mathrm{Inv_sb})$$

$$\mathrm{Kstress\ u0} = \left(1 + \frac{\mathrm{LKU0}}{(L+XL)^{\mathrm{LLODKU0}}} + \frac{W\mathrm{KU0}}{(W+XW+WLOD)^{W\mathrm{LODKU0}}} + \frac{P\mathrm{KU0}}{(L+XL)^{\mathrm{LLODKU0}} \cdot (W+XW+WLOD)^{W\mathrm{LODKU0}}}\right) \cdot (1 + TKU0 \cdot (T_{ratio} - 1))$$

$$\mathrm{Inv_sa} = \frac{1}{NF} \cdot \sum_{i=1}^{NF-1} \frac{1}{\mathrm{SA} + 0.5 \cdot L + i \cdot (SD + L)}$$

$$\mathrm{Inv_sb} = \frac{1}{NF} \cdot \sum_{i=1} \frac{1}{\mathrm{SB} + 0.5 \cdot L + i \cdot (SD + L)}$$

$$\rho_{ref} = \frac{\mathrm{KU0}}{\mathrm{Kstress_u0}} \cdot (\mathrm{Inv_sa_ref} + \mathrm{Inv_sb_ref})$$

$$\mathrm{Inv_sa_ref} = \frac{1}{\mathrm{SAREF} + 0.5 \cdot L}$$

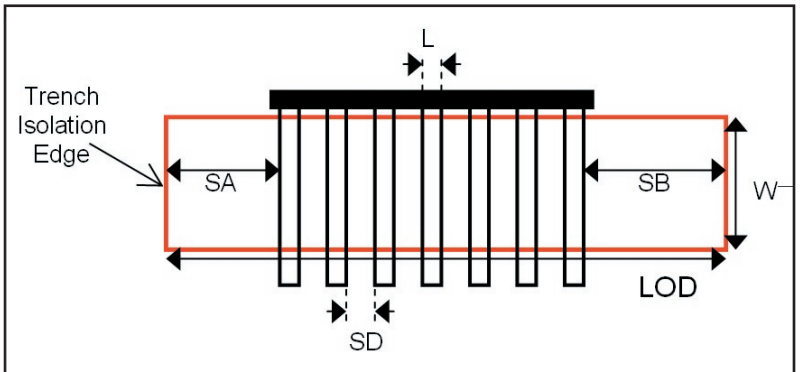
$$\mathrm{Inv_sb_ref} = \frac{1}{\mathrm{SBREF} + 0.5 \cdot L}$$

$$\mathrm{Kstress_vth0} = 1 + \frac{\mathrm{LKVTH0}}{(L+XL)^{\mathrm{LLODKVTH}}} + \frac{W\mathrm{KVTH0}}{(W+XW+WLOD)^{W\mathrm{LODKVTH}}}$$

Equation 5.

4. Conclusion

BSIM4 and HiSIM offer two different ways to account for the same physical phenomenom. The HiSIM model is physically-based but requires the computation of extra bias-dependent equations, which may be time-consuming when running large circuits. The Berkeley model is phenomenological and has no impact on simulation time because only some parameters are modified during pre-processing calculations (temperature- and geometry-dependent parameters). The accuracy of both models may vary significantly with STI processes.



$$LOD = SA + SB + NF \cdot L + (NF - 1) \cdot SD$$

Figure 4. Multi-fingers device geometry parameters.

Calendar of Events

July

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9	AM-LCD - Kogakuin Unv, Tokyo
10	AM-LCD - Kogakuin Unv, Tokyo
11	AM-LCD - Kogakuin Unv, Tokyo
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16	IMFED - Osaka, Japan
17	IMFED - Osaka, Japan
18	IMFED - Osaka, Japan
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21	NSREC - Monterey, CA
22	NSREC - Monterey, CA
23	NSREC - Monterey, CA
24	NSREC - Monterey, CA
25	NSREC - Monterey, CA
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August

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25	ISLPED - Soeul, Korea ISCS - San Diego, CA
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27	ISLPED - Soeul, Korea ISCS - San Diego, CA
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Bulletin Board

Silvaco Donates Software to University if Washington

Silvaco donated $2.4 million of software to the University of Washington College of Engineering to create an intellectual hub for advanced technology computer aided design (TCAD) research and development. The donated software simulates the behavior of semiconductor processes and devices using 3D field solvers to solve complex physics equations. The college of engineering faculty and graduate students will use this software to model reliability and performance of semiconductors as part of a joint development project between the University and Silvaco launched on May 19, 2003.

See Silvaco at NSREC

The IEEE Nuclear and Space Radiation Effects Conference (NSREC) presents the latest techniques for enhancing the performance of microelectronic devices and circuits that are used in radiation environments.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

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Hints, Tips and Solutions

Colin Shaw, Applications and Support Engineer

Q. My simulation fails because *SmartSpice* cannot find a binned model, what does this mean ?

Normally when a MOS model is extracted for a range of devices it is scaleable over the range of device geometries i.e. it is a continuous varying function over the required operating region for all device geometries. Sometimes there is too much variation in the output characteristics to be covered by one continuous model parameter set e.g. "straight" and "dog-bone" layout designs which contain very different electric field patterns. The total operating region is therefore broken up into sub-sections and a model produced for each of these subsets of device geometry. This is a binned model where each region is a different set of model card values for a smaller range of device properties like width, length and temperature. In this way a group of model card parameter sets can be used to cover a wide variation in say gate width and length variations not possible from a single scaleable model. In the simple case these bins are ranges of Width and Length transistor geometries that say what model card parameter set should be used. The only problem with this approach is a discontinuity at the boundary of one model set to another and can be thought of as trying to approximate a curve with a set of straight lines. Your error is because the device geometry is not covered by any of the specified ranges in the model library. Typically the binned model will have a model name of say nch.1, nch.2, nch.3 etc. and you device geometry is not allowed for in the say Lmin to Lmax range of any of these binned model sections.

New options functionality in SmartSpice

There are a number of .OPTIONS & variables in ***SmartSpice*** to allow the user to tailor the simulation environment to his needs. This becomes a bit confussing when there are so many options and they are inter-dependant and their influence on the circuit understood. To help the customer we have included a new variable in ***SmartSpice*** setoption

Since there are a number of option settings in ***SmartSpice*** that are not independent of each other we have created a new .OPTION optionset=<val> to simplify things. ***SmartSpice*** with the cell characterization values:

Optionset=<val>	Option used	Value
3	accurate	1
	cnode(cshunt)	1e-12
	ITL1	5000
	ITL2	5000
4	accurate	1
	cnode (cshunt)	1e-12
	conv	1
	accept	TRUE
	ITL2	5000

Optionset=3

This is recommended for transient analysis. This set of options helps to fix "Time step too small" problem (cnode=1.0E-12). Option ITL1=5000 allows more regular Newton iterations for the OP calculation. If the regular Newton iterations fail, ***SmartSpice*** automatically goes to the advanced stepping algorithm and uses 5000 iterations to find the OP. This set of options can be used if the transistor/diode models behave properly and the I/V curves are smooth.

Optionset=4

This is recommended for transient analysis to cover failure during .OP calculation due to slow convergence (ITL2=5000), helps to fix "Time step too small" during transient analysis (cnode=1.0E-12) and automatically accepts the solution during the advanced stepping in the OP calculation (ACCEPT). It also improves the I/V characteristics of the transistors and diodes when these curves are more irregular and uses DCGMIN parameter stepping (CONV=1) to fix internal device conductance's. This set of options is recommended for all cell characterization to cover convergence failures.

Q.How to detect bad models and solve the model problem ?

The construction of the device model is the fundamental building block on which the rest of the functionality is based. If the model card construction is poor then you can use the "gnode" option with a high value to get convergence but this just swamps the device with conductance masking the underlying problems and in some case just simulating a completely different circuit to the one intended. To detect a bad model you can include in the model card "PARAMCHK=1" this will highlight bad basic parameter values and the combination of parameters that lead to some equations of the model being outside or near their range limits. Another way is to include in the main input deck ".OPTIONS EXPERT". This allows a lot of errors to be reported and for every time point iteration so it is best to use this with a very limited simulation time to avoid too many repeated messages for each time point iteration. For the case where you have BSIM3v3 models ".OPTIONS EXPERT=779" is best giving more detail for this particular model and possible conflicts in the different aspects of the model to make sure it is overall consistent in specification. The input decks should also contain the setting ".OPTIONS CONV=1" which helps dc convergence by going straight to a more sophisticated stepping algorithm and giving more detail and suggestions should this stage fail to find an operating point.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

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